Patent Claims

1. Method for the production of a vertical MOS transistor,
- in which a mask (13) made of insulating material is formed on the main surface of a semiconductor substrate (11), which mask has an opening (130) in which the main surface is exposed,,
- in which a layer sequence (14), which has one layer (141,142,143) each for a lower source/drain region, a channel region and an upper source/drain region, is grown in the opening (130) by selective epitaxy, facets being formed on the edge of the layer sequence (14), so that the thickness of the layers (141,142,143) at the edge of the opening is less than in the middle,
- in which, after the layer sequence (14) has been formed, the side wall of the channel region (142) is exposed in such a way that the side wall of the lower source/drain region (141) remains essentially covered by the insulating material of the mask (131),
- in which a gate dielectric (16) which adjoins a surface of the channel region (142) is formed at the exposed side wall of the channel region (142),
- in which a gate electrode (170) is formed which adjoins the gate dielectric (16).

2. Method as claimed in claim 1,
in which the mask (13) comprises silicon oxide and/or silicon nitride at least at the surface.

3. Method as claimed in claim 1 or 2,
- in which the mask is formed from a first insulating layer (131) and a second insulating layer (132), the first insulating layer (131) being arranged at the main surface, and the second insulating layer (132) being arranged on the first insulating layer (131), it being possible to etch the second insulating layer (132) selectively with respect to the first insulating layer (131) and to the layer sequence (14),
- in which the lower source/drain region (141) ends essentially level with the first insulating layer (131),

- in which an opening that surrounds the channel region (142) is formed annularly in the second insulating layer (132),
- in which, after the gate dielectric (16) has been formed, the opening is filled with a conductive layer (17),
- in which the gate electrode (170) is formed by structuring the conductive layer (17).

4. Method as claimed in claim 3,
- in which the opening (15) in the second insulating layer (132) has an extension (150) at at least one side of the layer sequence (14), and island-like structures (132') are arranged in the region of the extension (150), so that the opening (15) has a grid-like cross-section in the region of the extension (150),
- in which the conductive layer (17) fills the opening (15) in the region of the extension (150) as well.

5. Method as claimed in one of the claims 1 to 4,
- in which the layer sequence (34) is structured in an annular shape and in which the annularly structured layer sequence (34) is provided with an insulating filling (39).